REMARKS

I. Informal Matters

Claims 1-13 are pending, and claims 5-13 have been withdrawn from further consideration in this application.

Applicant thanks the Examiner for acknowledging the Applicant's claim for foreign priority under 35 U.S.C. § 119(a)-(d) and for acknowledging receipt of the certified copies of the priority documents.

The Examiner objects to Figures 17-19 of the drawings. Applicant is submitting proposed drawing corrections to overcome this rejection, and respectfully requests the Examiner to approve these drawing corrections.

The Examiner objects to the Abstract of the disclosure. Applicant has amended the Abstract to overcome this objection and requests the Examiner to withdraw this objection accordingly.

The Examiner also objects to the specification as failing to provide proper antecedent basis for the claimed subject matter "constant current source" recited in claim 3.[1]

With regard to this objection, Applicant notes that the specification contains proper antecedent basis for the claimed subject matter. The "constant current source" of claim 3 is

clearly identified in the specification and in the drawings in the passage "The circuit of Fig. 3 has a MOS differential pair...which is driven by constant current Iss (=Io/2)" (Applicant's Specification, page 21, lines 12-16). The label "Iss (=Io/2)" appears clearly at the bottom of Figure 3.

Because the specification contains proper antecedent basis for the subject matter claimed in claim 3, Applicant respectfully requests the Examiner to withdraw the objection.

II. Claim Rejections under 35 U.S.C. § 112, second paragraph.

The Examiner rejects claims 1 and 3 under 35 U.S.C. § 112, second paragraph, as being incomplete for omitting essential elements. Applicant has amended claims 1 and 3 to more clearly recite the features of Applicant's invention, and notes that these amendments do not narrow the scope of the original claims 1 and 3, and do not exclude any equivalent structures as encompassed by the scope of the original claims. Claims 2 and 4 are allowable by virtue of their dependency on claims 1 and 3, respectively.

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[1] In the objection, the Examiner incorrectly references claim 4 as reciting the "constant current source." Applicant notes that this is a typographical error, and that the objection is clearly intended to refer to claim 3. Applicant responds accordingly.

III. Claim Rejections under 35 U.S.C. § 102(b)

The Examiner rejects claims 1-4 under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,602,509 to Kimura. Applicant respectfully traverses this rejection. Kimura does not disclose or suggest the combination of features of Applicant's invention as claimed in claims 1-4.

For example, one of the features of Applicant's invention as claimed in claim 1 is "drain electrodes of said first and second MOS transistors forming output terminals for outputting a signal to be subtracted." The Examiner alleges that circuit 3 (Figure 1, M51-M54) of Kimura is a "subtractor circuit for outputting a subtraction output signal i" (Office Action, page 4, paragraph 6). Applicant respectfully disagrees.

Applicant respectfully submits that the Examiner has misinterpreted Figure 1. That is, current i is not a subtraction output signal of the circuit M51-M54 as the Examiner alleges. Rather, current i is the output current of the current mirror circuit formed by M58-M59 (column 2, line 62-65). Even if, assuming *arguendo*, Kimura's circuit M51-M54 is a "subtractor circuit", current i is not its output.

Furthermore, assuming *arguendo* that circuit M51-M54 is a "subtractor circuit" as the Examiner alleges, the drain electrodes of M56 and M57 do not connect to that circuit, and therefore do not form "output terminals for outputting a signal to be subtracted" as required by claim 1.

Finally, Kimura does not disclose or suggest that circuit M51-M54 is a "subtractor circuit" as the Examiner alleges. Kimura describes this circuit only as a "cross-coupled quad cell" (column 2, lines 31-32). In fact, Kimura discloses that the "output current I_L of the quad cell is expressed by the equation... $I_L = aI (I_{D51} + I_{D52})$ where I_{D51} and I_{D52} are the drain currents of MOSFETs M51 and M52 respectively" (column 3, lines 1-24). Thus, Kimura's circuit M51-M54 is not a "subtractor circuit" as the Examiner alleges, but a circuit which performs addition of current signals.

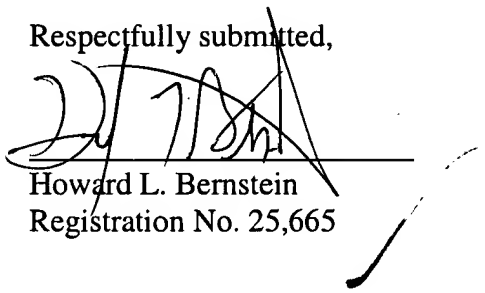
Claim 3 recites a feature of "drain electrodes of said first and second MOS transistors forming output terminals for outputting a signal to be subtracted." Thus, at least for the reasons discussed above with respect to claim 1, claim 3 is not readable on (i.e. is not anticipated by) Kimura.

In summary, because Kimura does not disclose, teach or even suggest, either explicitly or inherently, all of the limitations of claims 1-4, Kimura cannot anticipate these claims; that is, none of claims 1-4 are readable on Kimura's disclosure. Therefore, Applicant respectfully requests the Examiner to reconsider and withdraw this rejection.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

Applicant hereby petitions for any extension of time which may be required to maintain the pendency of this case, and any required fee, except for the Issue Fee, for such extension is to be charged to Deposit Account No. 19-4880.

Respectfully submitted,



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APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE ABSTRACT:

A voltage subtractor/adder circuit ~~comprises~~ has a differential pair having first and second MOS transistors. Gate electrodes of the first and second MOS transistors form input terminals for receiving an input differential voltage. Drain electrodes of the first and second MOS transistors form output terminals for outputting a subtraction output signal. Source electrodes of the first and second MOS transistors are commonly coupled to form an output terminal for addition output voltage. The sum of currents flowing through the first and second MOS transistors increases in proportion to the square of the input differential voltage. It is also possible to drive the differential pair by a constant current source. A level shifter may be provided for level-shifting the addition output voltage from the commonly coupled source electrodes.

IN THE CLAIMS:

The claims are amended as follows:

1. A voltage subtractor/adder circuit comprising:

a differential pair having first and second MOS transistors, gate electrodes of said first and second MOS transistors forming input terminals for receiving an input differential voltage, drain electrodes of said first and second MOS transistors forming output terminals for outputting

~~a subtraction output signal~~ a signal to be subtracted, and source electrodes of said first and second MOS transistors being commonly coupled to form an output terminal outputting a voltage to be added~~for addition output voltage~~; and

wherein the sum of currents flowing through said first and second MOS transistors increases in proportion to the square of said input differential voltage.

3. A voltage subtractor/adder circuit comprising:

a differential pair having first and second MOS transistors, gate electrodes of said first and second MOS transistors forming input terminals for receiving an input differential voltage, drain electrodes of said first and second MOS transistors forming output terminals for outputting a ~~subtraction output~~ signal to be subtracted, and source electrodes of said first and second MOS transistors being commonly coupled to form an output terminal for outputting a voltage to be added~~addition output voltage~~; and

a constant current source which drives said differential pair.